

# Writing Config Extractors

Navigating the challenges in extracting malware artifacts

Botconf 2024

#### About Us



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Souhail is a senior malware reverse engineer with the Intel 471 Malware Intelligence team. He's actively involved in reverse engineering malware and developing tools such as extractors and network protocol emulators to track malware and botnet activities.



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Miroslav is a senior security engineer with the Intel 471 Malware Intelligence team. He's actively involved in lots of "miscellaneous" stuff.



#### Agenda

- Introduction
- Lab setup TLP:AMBER+STRICT
- Part I General methodologies TLP:AMBER+STRICT
- Part II Regular expressions for code: RisePro hands-on TLP:GREEN
- Part III Using Unicorn and Capstone: Emotet hands-on TLP:GREEN
- Conclusion and Appendices TLP:GREEN



#### Introduction

- A malware's configuration is one of its most valuable assets.
- Samples typically come with a static configuration, sometimes minimal, that is set by the operator(s) before distribution.
  - Not expected to change unless explicitly updated or extended remotely.
- A malware config holds:
  - Command-and-Control (C2) servers.
  - Encryption keys and other configuration parameters.



#### Introduction

- Being able to extract elements of a malware's config allows defenders to:
  - Publish IOCs.
  - Emulate the malware's communications protocol (more IOCs).
  - Thwart or deeply inconvenience malware operators.
- For that reason, malware developers will:
  - Use obfuscation/encryption to conceal the config.
  - React to OSINT articles and config extractor scripts.



# Lab setup N/A in TLP:WHITE



#### Part I - General methodologies

#### N/A in TLP:WHITE



#### Part II - Regular expressions for code

- When and why you need to use regular expressions?
- Limitations of using regex to match code.
- Introducing Coderex.
- 2 Hands-on tasks.



## Regular expressions

- Sooner or later you will need to locate code in malware samples.
- For example:
  - To defeat encrypted stack strings.
  - To extract constants in the code.
  - To emulate instructions.

push	eax
push	1074 ; C2 port
call	sub_73BB4525
push	eax
lea	ecx, [ebp+var_60]
call	sub_73BBA315

Backconnect C2 TCP Port (Socks5SystemZ)

[ebp+var 1CA], 43595042h
ecx, ecx
[ebp+var 1C6], 47594D59h
[ebp+var_1C2], 53755E40h
[ebp+var_1BE], 1005147h
dword ptr [eax+eax+00000000h]
6C20:
<pre>/6C20: al, cl al, 27h ; ''' byte ptr [ebp+ecx+var_1CA], al ecx</pre>

Encrypted Stack Strings (RisePro)



## Why regex?

 Wildcard opcodes using a '.' operator re.compile(rb'\xB0.\xC3', re.DOTALL)

# MOV AL, XXh + RETN

- Alternation operator:
  - rb'\x75.|\x0F\x85....' # jnz short OR jnz near
- Ranges:



## Why regex?

Wildcard an arbitrary number of instructions:

rb'.{0,120}?' # Lazy match between 0 and 120 bytes of code

 Groups allow capturing data, especially at arbitrary offsets in dynamic buffers: rb'\xE8.{8,128}?\x68(?P<tcp\_port>..\x00\x00).{1,6}?\xE8' # PUSH tcp\_port



• Consume pattern as few times as possible and expand to yield the shortest match.

.{<mark>8</mark>,64}**?\xE**8

- Allows to retrieve the first occurrence in code.
- In most cases you'll want to use lazy quantifiers when wildcarding a range of bytes.



rb'\xE8.{8,128}?\x68(?P<tcp\_port>..\x00\x00).{1,6}?\xE8'

call 0x1000000 lea ecx, [edx+0x20] mov eax,DWORD PTR [ecx+0x4] push esi mov esi,DWORD PTR [ecx] push 0x1bb push 0x1 push esi call



rb'\xE8.{8,128}?\x68(?P<tcp\_port>..\x00\x00).{1,6}?\xE8'

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call

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• Consume as much as possible then backtrack to yield longest match.

.{8,<mark>64</mark>}\xE8

- Allows to retrieve the last occurrence.
- Can cause bugs when used incorrectly to extract artifacts.



rb'\xE8.{8,128}\x68(?P<tcp\_port>..\x00\x00).{1,6}\xE8'

call 0x1000000 lea ecx, [edx+0x20] mov eax,DWORD PTR [ecx+0x4] push esi mov esi,DWORD PTR [ecx] push 0x1bb push 0x1 push esi call



rb'\xE8.{8,128}\x68(?P<tcp\_port>..\x00\x00).{1,6}\xE8'

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Port was skipped



rb'\xE8.{8,128}\x68(?P<tcp\_port>..\x00\x00).{1,6}\xE8'

call 0x1000000 lea ecx, [edx+0x20] mov eax,DWORD PTR [ecx+0x4] push esi mov esi,DWORD PTR [ecx] push 0x1bb push 0x1 push esi call

Incorrect port in group tcp\_port != 0x01



rb'\xE8.{8,128}\x68(?P<tcp\_port>..\x00\x00).{1,6}\xE8'

call 0x1000000 lea ecx, [edx+0x20] mov eax,DWORD PTR [ecx+0x4] push esi mov esi,DWORD PTR [ecx] push 0x1bb push 0x1 push esi call

Incorrect port in group tcp\_port != 0x01



#### Lazy vs. Greedy

- Opt for lazy mode when regex is FP prone:
  - The pattern after the range quantifier is too generic.
- The choice of which mode heavily depends on the specific use-case.



- Stack string decryption loop in the RisePro stealer.
- We want to match and extract the <u>XOR key</u> and <u>string length</u>.
- Decryption process:
  - Add the current index to the initial XOR key: value is 0x27 (changes between samples).
  - XOR byte on stack, increment the index and compare the length.

mov	[ebp+var 1CA], 43595042h
xor	ecx, ecx
mov	[ebp+var_1C6], 47594D59h
mov	[ebp+var_1C2], 53755E40h
mov	[ebp+var_1BE], 1005147h
nop	dword ptr [eax+eax+00000000
100 45	6620.
loc_45	
mov	al, cl
mov add	al, cl al, 27h ; '''
mov	al, cl
mov add xor inc	al, cl al, 27h ; ''' byte ptr [ebp+ecx+var_1CA],
mov add xor inc	<pre>al, cl al, 27h; ''' byte ptr [ebp+ecx+var_1CA], ecx</pre>



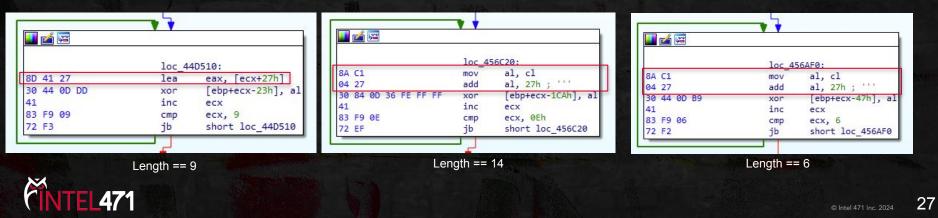
- Decryption process:
  - Add the current index to the initial XOR key: value is 0x27 (changes between samples).
  - XOR byte on stack, increment the index and compare the length.
- Samples has 2 equivalent variants of how the key is calculated: <u>LEA</u> vs. <u>MOV + ADD</u>

	loc 4	4D510:		loc_4	56C20:		loc 4	56AF0:
8D 41 27	lea	eax, [ecx+27h]	8A C1	mov	al, cl	8A C1	mov	al, cl
30 44 0D DD	xor	[ebp+ecx-23h], al	04 27 30 84 0D 36 FE FF FF	add	al, 27h ; '''	04 27	add	al, 27h ; '''
41	inc	ecx	30 64 00 36 FE FF FF	xor inc	<pre>[ebp+ecx-1CAh], al ecx</pre>	30 44 0D B9	xor	[ebp+ecx-47h], a
83 F9 09	cmp	ecx, 9	83 F9 ØE	cmp	ecx, 0Eh	41	inc	ecx
72 F3	jb	short loc_44D510	72 EF	ib	short loc_456C20	83 F9 06 72 F2	cmp ib	ecx, 6 short loc 456AF0



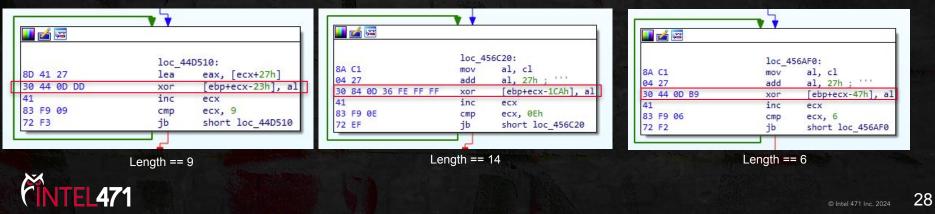
re.compile(

rb'(\x8A\xC1\x04|\x8D\x41)(?P<key>.)'



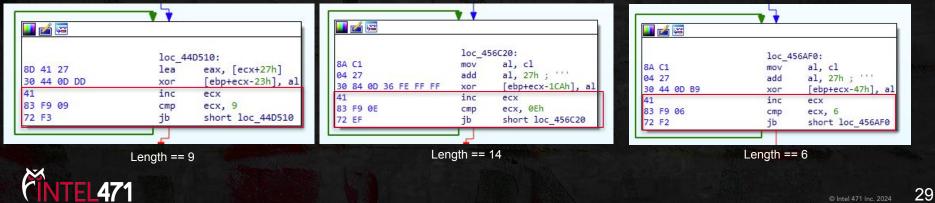
re.compile(

rb'(\x8A\xC1\x04|\x8D\x41)(?P<key>.)' rb'\x30(\x44\x0D.|\x84\x0D....)'



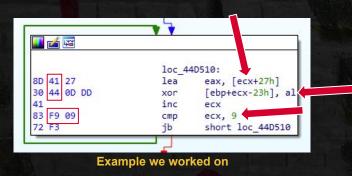
#### re.compile(

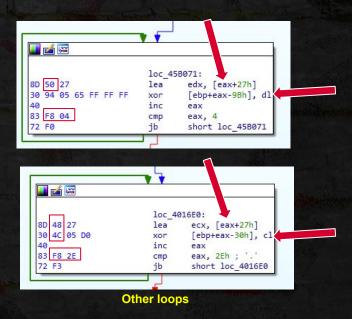
rb'(\x8A\xC1\x04|\x8D\x41)(?P<key>.)' rb'\x30(\x44\x0D.|\x84\x0D....)' rb'\x41' rb'\x83\xF9(?P<len>.)' rb'\x72' ), re.DOTALL)



• The regular expression we wrote does not match all decryption loops.

- Some loops use registers we did not take into account.
- Regex needs to be improved to match these blocks.
- Code is volatile. Regex is better suited for text.





- The x86 and x86-64 instruction sets are tricky. For example:
  - A lot of instructions support a memory operand as either src or dest.
  - But never two memory operands.
  - Requires the instruction to be encoded two different ways.
  - When both operands are registers, the two encodings become equivalent.
  - The choice of which encoding to use is left to the assembler.
- A variance to consider.

89 c6	mov	esi, ea	x ;	MOV	r/m32	,	r32
8b f0	mov	esi, ea	х ;	MOV	r32	,	r/m32



- Stack-frame indexing:
  - Usually by the stack-frame base pointer EBP e.g. [EBP-0x0C].
  - But ESP could be used as a base e.g. [ESP+0x0C].
    - Frame-Pointer Omission optimization.
- An additional variance to consider.

C7	45	98	94 9	8 89	91	mov	dword	ptr	[ebp-68h],	91899894h	C7	84	24	75	01 (	00 00	0 ED	AE	94	6E	mov	dword	ptr	[esp+175h],	6E94AEEDh
C7	45	9C	8F A	B AE	AC	mov	dword	ptr	[ebp-64h],	ØACAEAB8Fh	C7	84	24	79	01 (	00 00	0 50	CD	EA	BØ	mov	dword	ptr	[esp+179h],	0B0EACD5Ch
C7	45	AØ	B8 9	5 80	A7	mov	dword	ptr	[ebp-60h],	0A78095B8h	C7	84	24	7D	01 (	00 00	0 FD	B6	7F	18	mov	dword	ptr	[esp+17Dh],	187FB6FDh
C7	45	A4	80 B	3 AE	A2	mov	dword	ptr	[ebp-5Ch],	ØA2AEB3BØh	C7	84	24	81	01 (	00 00	0 C8	60	91	D9	mov	dword	ptr	[esp+181h],	0D99160C8h
C7	45	A8	B5 9	6 AF	BØ	mov	dword	ptr	[ebp-58h],	0B0AF96B5h	C7	84	24	85	01 (	00 00	0 B9	58	58	E4	mov	dword	ptr	[ <mark>esp</mark> +185h],	0E45858B9h
C7	45	AC	A3 A	D AA	B7	mov	dword	ptr	[ebp-54h],	0B7AAADA3h	C7	84	24	89	01 (	00 00	0 88	4C	32	2B	mov	dword	ptr	[ <mark>esp</mark> +189h],	2B324C88h
C7	45	BØ .	AA B	0 B6	B4	mov	dword	ptr	[ebp-50h],	0B4B6B0AAh	C7	84	24	8D	01 (	00 00	0 01	8C	76	1A	mov	dword	ptr	[esp+18Dh],	1A768C01h
C7	45	B4	7E 9	3 91	B1	mov	dword	ptr	[ebp-4Ch],	0B191937Eh	C7	84	24	91	01 (	00 00	0 10	BC	3C	B6	mov	dword	ptr	[esp+191h],	0B63CBC10h
C7	45	B8	A3 8	4 67	A8	mov	dword	ptr	[ebp-48h],	0A86784A3h	C7	84	24	95	01 (	00 00	0 60	2A	E7	E9	mov	dword	ptr	[ <mark>esp</mark> +195h],	0E9E72A6Dh

Pikabot (EBP-based frame indexing)

Pikabot (ESP-based frame indexing)



- What seemed to be a trivial regex to write would end up:
  - Taking time to find variants and to anticipate any future code changes.
  - Gathering technical debt.

rb'\xC7\x87...\x00\x01\x00\x00\x00' # mov dword ptr [edi+20D8h], 1 rb'\xC7[\x80-\x87]...\x00\x01\x00\x00\x00' # mov dword ptr [edi+20D8h], 1

Example commit 1: Builds appeared that would use other registers than EDI



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	rb'\xC7\x87\x00\x01\x00\x00\x00' # mov dword ptr [edi+20D8h], 1
+	rb'\xC7[\x80-\x87]\x00\x01\x00\x00\x00' # mov dword ptr [edi+20D8h], 1
	Example commit 1: Builds appeared that would use other registers than EDI
-	<pre>rb'(\xC7\x45.(?P<key_0>))' # mov [ebp+var_20], 0FCA00CAEh; Additional RC4 key rb'(\xC7\x45.(?P<key_1>))'</key_1></key_0></pre>
+ +	<pre>rb'(\xC7(\x45. \x85)(?P<key_0>))' # mov [ebp+var_20], 0FCA00CAEh; Additional RC4 key rb'(\xC7(\x45. \x85)(?P<key_1>))'</key_1></key_0></pre>

Example commit 2: In some samples, functions had a larger variable space.



- What seemed to be a trivial regex to write would end up: •
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  - Gathering technical debt.

	TRANSFE STRANSFE					
	-	rb'\xC7\x87\x00\x01\x00\x00\x00	# mov dwa	rd ptr [edi+20D	8h], 1	
	+	rb'\xC7[\x80-\x87]\x00\x01\x00\x00	\x00' # mov	dword ptr [	edi+20D8h], 1	
	The second	Example commit 1: Builds appeared that would	use other regi	sters than EDI	in man and an man	
₹3		rb'(\xC7\x45.(?P <key_0>))' # mov [</key_0>	ebp+var_20],	0FCA00CAEh; Addi	tional RC4 key	
-		rb'(\xC7\x45.(?P <key_1>))'</key_1>				
+		rb'(\xC7(\x45. \x85)(?P <key_0>))'</key_0>	# mov [eb	p+var_20], OFCAG	OCAEh; Additional	RC4 key
+		rb'(\xC7(\x45. \x85)(?P <key_1>))'</key_1>				68
		Example commit 2: In some samples, function	ns had a large	r variable space.		
				The second		
			1 Cart			4
		rb'(?P <emu_end>\x75.)'</emu_end>	# jnz	short loc_15	i0	South Real
	+	rb'(?P <emu_end>(\x75. \x0F\x85))'</emu_end>		# jnz	short loc_150	

Example commit 3: The branch target could be farther. 'JNZ near' is possible.



#### Introducing Coderex

- Experimental tool we developed to tackle these challenges.
- Generates generic regular expression given a stream of code (x86 or x86-64).
- Relies on the iced assembler/disassembler (https://github.com/icedland/iced).
- Released today on: <u>https://github.com/intel471/coderex</u>



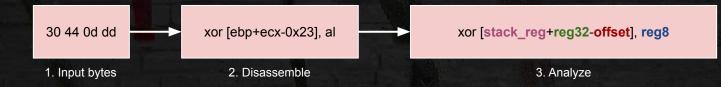


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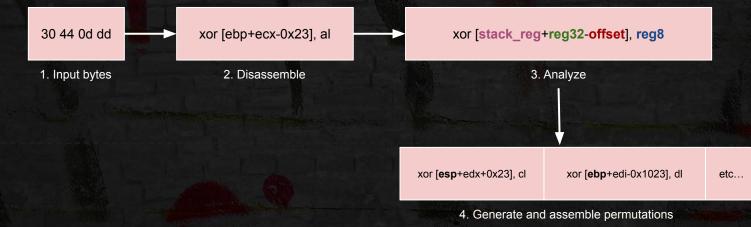


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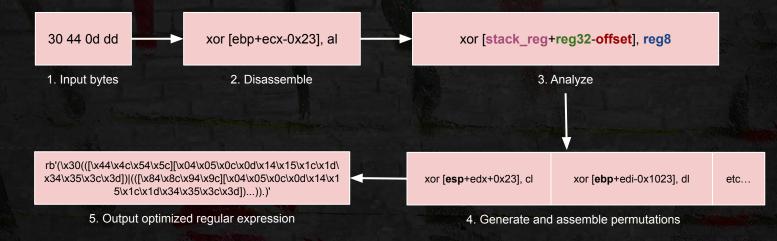


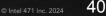
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## Coderex: Demo

- Generic x86 regular expression for:
  - 21 C0 and eax, eax
- Visualize the regular expression using: <u>https://regexper.com/</u>
- Assemble a few variants from the regex.
  - Online assembler/disassembler: <u>https://defuse.ca/online-x86-assembler.htm</u>
  - Notice that:
    - Coderex detected that the source and destination are the same.
    - Both r/m32 and m32/r encodings are generated.



## Coderex

- In some cases we'd want to modify the regexes:
  - To add in groups.
  - Wildcard offsets.
- We need to understand the assumptions the tool makes.



#### Immediates

• Immediate values are preserved.



# Branching

- Call targets are wildcarded.
- For relative jumps, both *short (1 byte)* and *near (4 bytes)* variants are generated.

# call 01001400h rb'(\xe8....)'

# jmp near ptr 01001400h rb'(((\xe9...)|\xeb).)'



# Memory (Direct)

• Direct memory accesses are wildcarded.

# mov dword ptr ds:[1000h],1337h ; '.{10}' rb'(\xc7\x05....\x37\x13\x00\x00)'

> # call dword ptr ds:[<mark>2000h</mark>] ; '.{6}' rb'(\xff\x15....)'

> # jmp dword ptr ds:[3000h] ; '.{6}' rb'(\xff\x25....)'



# Memory (Displacement)

- Displacements are trickier to handle.
- Base address assumed for code/memory:
  - 0x100000 by default.
  - Only displacements above or equal will be wildcarded.



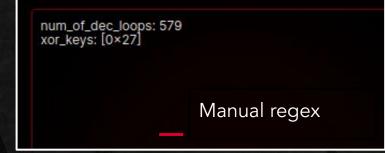
# Memory (Displacement)

• For code that accesses low memory addresses. For example:

- Shellcode loaded into a low address segment in IDA Pro.
- Override default base address using '-d'.



#### Coderex: hands-on







## Part III - Unicorn and Capstone.

• Objective: write an Emotet config extractor for C2 servers.

- Introduce the Unicorn emulation engine:
  - To write config extractor for a single C2.
  - 1 Hands-on task.
- Introduce the Capstone disassembler engine:
  - To improve the extractor to automatically extract all C2s.
  - 2 Hands-on tasks.



# Unicorn engine

- Lightweight and multi-architecture CPU emulator framework based on QEMU.
- Interprets machine instructions within a software-based context to replicate the behavior of a CPU.
- Actively maintained and widely adopted by the malware community.
- Easy to install: "pip install unicorn"



www.unicorn-engine.org



from unicorn import \* from unicorn.x86\_const import \*

- unicorn module:
  - Contains the "Uc" emulation class.
- x86\_const module:
  - Defines x86 and x86-64 constants for registers and instructions.





# code to be emulated
X86\_CODE32 = b"\x41\x4a" # INC ecx; DEC edx

# memory address where emulation starts
ADDRESS = 0x1000000

- Initialize the instructions to emulate.
  - 41 INCECX
  - 4A DEC EDX
- Setup address where they will be written to in the emulator's memory.



# Initialize emulator in X86-32bit mode
mu = Uc(UC\_ARCH\_X86, UC\_MODE\_32)

- Instantiate an Unicorn emulator object "Uc" for the target architecture.
  - UC\_ARCH\_X86: The x86 CPU architecture.
  - UC\_MODE\_32: The 32-bit CPU mode.
    - UC\_MODE\_64 to emulate 64-bit code.



# map 2MB memory for this emulation mu.mem\_map(ADDRESS, 2 \* 1024 \* 1024)

# write machine code to be emulated to memory mu.mem\_write(ADDRESS, X86\_CODE32)

- In a fresh emulator, all memory is unmapped.
  - Raises an exception when accessed.
- Call "mem\_map" to map memory with:
  - The memory address to map in the address space.
  - The memory size in bytes aligned to page boundary (4096).
  - The permissions, by default RWX.
- Memory can then be written to using mem\_write.



# initialize machine registers
mu.reg\_write(UC\_X86\_REG\_ECX, 0x1234)

mu.reg\_write(UC\_X86\_REG\_EDX, 0x7890)

- Initialize registers affected by calling "reg\_write":
  - $\circ$  ECX = 0x1234
  - $\circ$  EDX = 0x7890
- All registers are initially 0.



# emulate code in infinite time & unlimited instructions mu.emu\_start(ADDRESS, ADDRESS + len(X86\_CODE32))

- Call "emu\_start" with the arguments:
  - Start address of the code: 0x1000000.
  - End address: 0x1000002.
- "emu\_start" synchronously emulates the code.
  - Only returns when the end address is reached or an exception occurs.
  - Can get stuck indefinitely or for a long time.



# emulate code in infinite time & unlimited instructions mu.emu\_start(ADDRESS, ADDRESS + len(X86\_CODE32))

"emu\_start" accepts 1 of these 2 arguments to control the emulator's execution.

- "count": A number that limits the individual instructions to execute.
- "timeout": The maximum runtime of the emulation in nanoseconds.
  - 10 milliseconds: 10 \* UC\_MILISECOND\_SCALE
  - 10 seconds: 10 \* UC\_SECOND\_SCALE



•

# emulate code in infinite time & unlimited instructions mu.emu\_start(ADDRESS, ADDRESS + len(X86\_CODE32))

- Emulation stops at whichever comes first:
  - The instruction pointer reached the end address.
  - The "count" or "timeout" has expired.
  - An exception occured.



# now print out some registers
print("Emulation done. Below is the CPU context")

r\_ecx = mu.reg\_read(UC\_X86\_REG\_ECX)
r\_edx = mu.reg\_read(UC\_X86\_REG\_EDX)
print(">>> ECX = 0x%x" %r\_ecx)
print(">>> EDX = 0x%x" %r\_edx)

- After emulation:
  - $\circ$  ECX = 0x1234 + 1 = 0x1235
  - $\circ$  EDX = 0x7890 1 = 0x788f



• To learn more about the engine's capabilities, find examples at:

<u>https://github.com/unicorn-engine/unicorn/blob/master/bindings/python/sample\_x86.py</u>



#### Case-study: Emotet

- In May 2022, Emotet updated its C2 config storage method. •
  - Callback table of 64 functions. 0
  - Each function decodes and returns the C2 IP and port. 0
  - The C2 can be a decoy. 0
  - The table is walked until a functional C2 is found. 0
- Callback functions: •
  - 1 basic block.
  - Mostly junk code. 0
  - Uses XOR to calculate the C2 IP and port. 0

40	callback_table[48]	= (int64)sub_18001A2EC;
41	callback_table[5] =	= (int64)sub_180025204;
42	callback_table[23]	= (int64)sub_180018968;
43	callback_table[39]	= (int64)sub_18001EAE8;
44	callback_table[54]	= (int64)sub_1800231CC;
45	callback_table[13]	= (int64)sub_1800245F8;
46	callback_table[56]	= (int64)sub_180011B20;
47	callback_table[32]	= (int64)sub_18000D088;
48	callback_table[28]	= (int64)sub_18002071C;
49	callback_table[42]	= (int64)sub_1800123A8;
50	callback_table[29]	= (int64)sub_180005240;
51	callback_table[44]	= (int64)sub_18001C61C;
52	callback_table[38]	= (int64)sub_18002676C;
53	callback_table[40]	= (int64)sub_18001A010;

#### Callback table being initialized





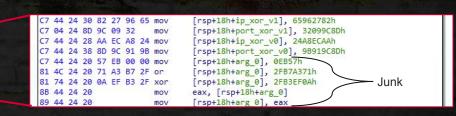
@ Intel 471 Inc 2024

	248,13	MIA25C proc mean
	var_10 var_C= arg_0= 1p_sor 1p_sor	nr_vi+ despri ptr -38h despri ptr -38h despri ptr -38h despri ptr -38h vite despri ptr -38h vite despri ptr -38h
	pert_x	sr_elle dword gtr 28h
48 83 8C 18	110	rsp, 10b
17 44 24 68 35 1A 88 39 88 EB	MDN NOT	[rspeidbecar_10], LABAN
C ER CL	-	re, ros
99 44 24 BC	mer-	[rsp+LSh+var_C], eas
T 44 24 28 47 DF 88 00		[rsp+100+arg_0], 00r47%
30 37 C5 25 43 30 54 24 20	BOV BOY	ess, 43(55537h eds, [rep+10+erg_0]
F7 62	and	eds
C1 EA (05	she	eds, 3
99 54 24 20	-	[rsps18brarg_0], edu
51 44 24 28 47 C9 88 00 51 74 24 28 65 C7 84 00		[rsp+lSh+arg_0], BC34Th [rsp+lSh+arg_0], 4C76Sh
10 44 24 20 00 CF 04 00	BDV .	was, [rap+10h+arg_0], +Lroon
29 44 24 28	80.4	fragetoheurg 01, and
		Lada mouth Ten Ten IV assessment
CT 84 24 80 9C 89 32 CT 44 24 28 44 5C 48 24	BOY .	(rspillingarl_our_s1), t2895020. (rspillinig_sor_v0), 244860400
C7 44 24 38 80 9C 91 98		(rap+10h+port_xor_w0), 10010000h
CT 44 24 28 57 25 88 00	804	[rap+10h+arg 0], 00057h
01 4C 24 20 71 AD 87 27		[rap+100+arg_0], 2007A371h
01 74 24 28 84 6F 83 2F 88 44 24 28	HEN .	(rsp+10h+arg 0], 1F201F00h eas, [rsp+10h+arg 0]
00 44 25 20 00 44 25 20	-	(rsp+18hterg 0], eas
88 42 24 28	-	ers, [rapilShrip and v0]
00 44 24 30	MON .	eas, [rap41894ip apr v1]
33 CB	xor	ecs, eax ; ecx = 1p_cor_v0 = 1p_sor_v1 ; ecx <= 12-bit 19v4 address
41 88 62	-	<pre>; ecx &lt;= 32-bit 1Pv4 address [r8], ecx ; Stored to pointer output parameter</pre>
CT 44 25 28 38 F1 88 80	801	[rsp+100+arg_0], ##1000
81 74 24 28 29 80 28 89	REF	[rsp+180+arg_0], mms20000min
61 74 24 20 55 C6 85 61	807	[rap+10h+erg_0], #1000005h
01 74 24 28 FL 82 24 08 08 44 24 28	NOT BOY	[rsp+13h+erg_0], 0002482f1h ess, [rsp+18h+erg_0]
00 44 24 28	BOY	[rup+1Sh+arg 0], eas
88 42 24 38	-	ecs. [rsp+180+port wor we]
88 84 25	-	eas, [rspelmeport_sor_v1]
53 CB	RET	ecs, eas ; ecs = pert_sor_w0 ^ pert_sor_v1
66 25 49 52 24	809	ean, 24924825h ; jank
41 89 48 64	mpir	[r8+4], ecs ; Stored to pointer output parameter
C7 44 24 28 32 4A 68 60	acu thr	[rsp-lib-arg_0], 4830h
C1 66 26 28 89 81 78 24 28 81 48 84 60		[rsp+120+arg_0], # [rsp+120+arg_0], #D0114818
68 4C 24 28	mer.	ecs. [rspilDitorg 8]
P7 E1	well.	RCS .
28 CA	100	scs, adc
01 E9 99 CA	shr add	ecs, 1 scs, eds
	skr	eca, 1
89 42 24 28	-	[rsp+10h+arg_0], etc
08 44 24 28	mon .	ess, [rspelSterg_0]
C1 E8 03 59 44 24 28	242	can, 3
09 44 24 28 01 74 24 20 55 76 58 35		[rsp+L0h+arg_0], ass [rsp+L0h+arg_0], 309076258
08 44 24 28	801	eas, [repelifyeorg.#]
89 44 24 28	MON .	[rsp+180+arg 0], eas
48 83 CA 18	odd	rap. 180
C3 .	rets	

		83 44			36	14	00	00	sub mov	rsp, 18h [rsp+18h+var 10], 1A36h
	1.5.1.5	CO	2.4			-			xor	eax, eax
		8B	C1						mov	r8, rcx ; Accepts a single argument in RCX
	1000	44		0C					mov	[rsp+18h+var C], eax
	C7	44	24	20	47	DF	00	00	mov	[rsp+18h+arg 0], 0DF47h
	<b>B</b> 8	3F	C5	25	43				mov	eax, 4325C53Fh
1	8B	54	24	20					mov	edx, [rsp+18h+arg 0]
	F7	E2							mul	edx
	C1	EA	05						shr	edx, 5
	89	54	24	20					mov	[rsp+18h+arg_0], edx
	81	44	24	20	47	C9	00	00	add	[rsp+18h+arg_0], 0C947h
	81	74	24	20	66	CF	04	00	xor	[rsp+18h+arg_0], 4CF66h
	8B	44	24	20					mov	eax, [rsp+18h+arg_0]
	89	44	24	20					mov	[rsp+18h+arg_0], eax



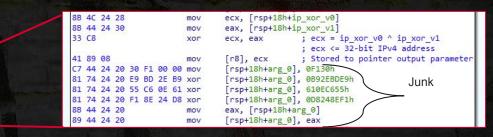
2	a_10001425C proc sear-
P	ort_sor_vi= deord ptr -38h
	ar_10+ dword ptr -10h ar 5+ dword ptr -8Ch
	a de deard ptr a
1	p sor vie dword pir 18h p sor vie dword pir 18h
	ort_wor_wie dword gtr 20h
	ab rsp, sin
C7 44 24 68 36 1A 88 80 m	
	er es, ess
59 44 24 RC	ev (rapil@hevar.Cl. est
CT 44 24 28 47 DF 88 00 m	
	ean, 43256537h
	ow sds. [repeldveorg_0]
C1 EA 05 5	er edu, u
	en [rsps18brarg_0], eds
51 44 24 28 47 C9 88 00 s 51 74 24 28 65 CF 84 00 x	dd [rap+15h+arg_0], 80347h
	or [rap+10h+arg_0], 4CP66h ow waw, [rap+10h+arg_0]
00 44 34 36 m	formation and and
C7 44 24 38 82 27 98 65 m C7 84 24 80 90 09 12 m	
C7 84 24 80 9C 89 32 8 C7 44 24 28 AA 5C 48 24 8	w (rsp+180+part_sor_s1), 12000000 w (rsp+180+12_sor_v0), 24488040
CT 44 24 38 83 9C 93 98 m	
C7 44 24 28 57 25 88 00 m	ov [rap+10h+arg_0], #0057h
01 4C 24 20 71 A3 87 27 p 01 74 24 20 0A 6F 83 27 x	
EL 74 24 20 64 67 83 27 K	
45 44 35 38	(contributers al. en
88 40 24 28	
08 44 24 38 m 33 68 x	
41 28 92	
C7 44 25 28 38 F1 88 88 8	te [rsp+100+erg_0], sr1000
81 74 24 28 29 80 28 89 x	er [rspt18htarg_0], ##9200003h
61 74 24 20 55 C6 00 61 x 61 74 24 20 F1 60 24 00 x	or [rsp+10h+erg_0], 85000005h or [rsp+15h+erg_0], 000246271h
	te ess, [rep+10h+erg.4]
	tw [rup+10h+arg 0], eas
88 4C 25 38 m	
	<pre>iv eas, [rspelDeport_wor_v1] ir ecs, eas</pre>
	ee ees, 24924825h ; junk
41 29 40 04	De [r8+4], ecs ; Stored to pointer output parameter De [rap+13h+arg 0], 4830h
C1 6C 25 28 89 5	fragetimearg 0], #
51 74 24 28 81 AS 84 80 w	er [rsp+18h+arg_0], #DSDAR#18
68 4C 24 28 *	
	d ecs ib scs. edc
a 10	er er l
	ož scu, edu
CI E9 08 S	ter ecs, # ter [rsp+18bearg 0], ecs
	te (rsprinting 0], etc
C1 58 03 3	eas, 3
	ce [rsp+10b+erg_0], ess
21 74 24 20 25 76 58 35 x	or [rap+10h+arg 0], 100076058 on eas, [rap+10h+org 0]
	(rsp+180-earg 0], eas
	64 rsp. 180
C3	cta .



- XOR parameters are written to the stack.
  - IPv4 parts: ip\_xor\_v1, ip\_xor\_v2
  - Port parts: port\_xor\_v1, port\_xor\_v2



	248_15	MIA20C proc mean-
		r_vl= deord ptr -18h
		dward ptr -100
	Arg. Br	deard ptr #
	Ip apr	v8s shord ptr 18h v1s shord ptr 18h
	ip_sor, port_o	v2= dword ptr 180 r_w8= dword gtr 200
48 83 85 18	110	rap, tiln
C7 44 24 68 36 1A 88 80	MDW NDY	[rep+12b+var_12], 1Abin
AC BB CL	and the second	rea, eox re, rox
59 44 24 RC	BOY .	[rspilShever C], est
CT 44 24 28 47 DF 88 00		[rap+10h+arg 0], 00747h
50 3F C5 25 43 80 54 28 20	BC4 BCV	ess, 43156537h eds, [rep+10+erg.#]
67 62	and	eds (reperment_e)
C1 EA 05	shr	eds, 3
55 54 24 20	-	[rspallhearg 0], eds
51 44 24 28 47 C9 88 00 51 74 24 28 55 C7 84 00		(rap+Löhtarg_0), 80347h
10 44 24 20 05 CF 04 00	BDV .	[rsp+l0h+arg_0], 4CP66h waw, [rsp+l0h+arg_0]
09 44 24 28	BDw.	[rsp+10h+arg_0], say
C7 44 25 38 82 27 86 65		[rsp+18h+1g_mor_s1], 65682782h
C7 84 24 80 90 89 52 C7 44 24 28 44 50 48 24	BOY.	(rsp+180+part_sor_s1), 128990808 (rsp+180+5p_sor_v8), 24488040
C7 44 24 38 80 9C 91 98		(rsp+10h+port_xor_w8), 98310C60h
C7 44 24 28 57 25 88 00	mov.	[rap+10hearg_0], 80057h
01 4C 24 20 71 AD 87 2F		[rsp+10b+srg_0], 2007A371h
01 74 24 20 0A DF 83 2F	NOT THE	(rsp+100+arg 0], 2F221F000 eas, [rsp+100+arg 0]
10 44 25 20 10 44 25 20	-	(rspet20rearg 0], eas
00 45 29 20 00 44 26 30	101	
55 44 24 50 53 CB	NEW	eas, [rap410+ip_sor_v1] ecs, eax ; ecx = ip_sor_v0 = ip_sor_v1
		; ecx c+ 32-bit 1904 address
41 88 62	86+	[r#], ecs ; Stored to pointer output parameter
C7 44 25 20 30 F1 80 90 51 74 26 20 F9 80 27 89		[rsp120+arg_0], #F1200h [rsp120+arg_0], #F5200003h
51 74 74 20 55 Ch Mr. 61	100	[rsp+10h+erg_0], Eleccess
\$1 74 24 28 FL 85 34 D8	SET	[rap+18h+arg_0], 000246271h
00 44 24 20 00 44 24 20	BC+	ess, [rsp+100+erg_0] [rsp+100+erg_0], ess
er 77 en en	BCY .	fisherman [14] and
08 84 24	-	eas, [rspelmeport_sor_v1]
33 CB	REF	ecs, eas ; ecs = part_sor_w0 ^ part_sor_w1
55 25 49 52 24	809	ess, 24924825h ; jank
41 89 40 64	MOV .	[r8+4], ecs ; Stored to pointer output parameter [rap+Lin+arg_0], 4830h
	uhr .	[rsp+130+arg 0], #
81 78 24 28 81 AS 88 80		(rsp+180+arg_0, #0504818
68 4C 24 28	MON .	ecs, [rsps18ssarg_8]
20 CA	and a	ecs, eds
01 59	abr	ecs, 1
	add	scs, eds
	shr	ecs, I
	-	[rspt18htarg_0], etc. ess. [rspt18htarg_0]
C1 58 93	244	eas, 3
59 44 24 28	BCN .	[rap+10h+arg_0]; sax
21 74 24 20 55 76 58 35		[rup+10h+arg_0], 3090r6258
08 44 24 29 89 44 26 29	and of the local division of the local divis	sas, [rsp+18h+arg_0], sas
48 83 CA 18	and d	rsp. 180



- ip\_xor\_v0 ^ ip\_xor\_v1 = IPv4 in network-byte order.
- Stored to the output argument in <u>offset 0</u>.



	#_13881A25C proc mean	
	ort_sor_si= deord ptr -lik	
	r_10+ dword ptr -10h r_5+ dword ptr -8Ch	
	a ne deard one a	
	sor vie shord ptr 18h sor vie shord ptr 18h	
	stor_v1= dword ptr 18h	
	rt_cor_ves daors gtr 185	
48 83 DC 18	a rsp, tilt	
C7 44 24 68 35 1A 88 99		
AC ES CL	er sax, dax	
59 44 24 RC	w (rspillhever C), eas	
CT 44 24 28 47 DF 88 00	w [rsp+100+arg_0], 00/47h	
00 37 C5 25 43 00 54 24 20	w eds. [csp+10+ecs #]	
F7 62	w eds, [repelifieorg_0]	
C1 EA 05	eda, a	
59 54 24 20	m [rspel@bearg_0], eds	
51 44 24 28 47 C9 88 00 51 74 24 28 55 CF 84 00		
01 74 24 20 00 CF 64 00	was, Inspelificers #1	
09 44 24 28	w [rup+10hearg_0], say	
C7 44 25 38 82 27 86 65	<pre>im [/sp+18h+1p wor w1], 658m2782h</pre>	
CT 84 24 80 9C 89 32 CT 44 24 28 44 5C 48 24	<pre>w (rsp+18h+par1_aor_s1), 128490000 w (rsp+18h+1p_aor_v8), 24488044h</pre>	
C7 44 24 38 80 9C 91 98		
CT 44 24 28 57 25 88 00	w [rap+10hearg_0], acos7h	
01 4C 24 20 71 AD 87 27		
01 74 24 28 84 6F 83 2F 88 44 24 28	<pre>ir (rsp+100+arg 0], 2F201F000 is eas, [rsp+100+arg 0]</pre>	
89 44 25 29	(rsprishterg 0], eas	
88 42 24 28	ecs, [rapelSheip_sar_v0]	
	<pre>w eas, [rspil@vip_mor_vi] w ecs, eax ; ecs = ip_wor_v0 * i</pre>	100 C 100
33 68	<pre>r ecs, eax ; ecx = ip_cor_v0 * 1 ; ecx &lt;= 32-bit 1Pv4</pre>	p_spr_vi
41 88 92	ie [r#], ecs ; Stored to pointer o	atput parameter
C7 44 25 28 38 F1 88 80		
81 74 24 28 29 80 28 89 61 74 24 28 55 C6 85 61	r (rsp+100+erg_0), 0052000030	
01 74 24 28 FL 05 24 00	[rap+18h+erg_0], 000246271h	
	eas, [rap+10+arg_0]	
IB 4C 25 38	ecs, [rsp+18+port_xor_y8]	
88 84 24	in eas, [rspelimeport_mon_wi]	
53 CB	r ecs, eas ; ecs = pert_sor_s0 *	pert_wor_v1
55 25 49 52 24	w www. 24924925h ; junk	
41 29 40 04	<pre>in [r8+4], ecs ; Stored to pointer c</pre>	artest parameter
C7 44 24 28 32 44 88 99	a [rap+ilh+arg_0], 4x10h	
C1 6C 25 28 89	rsp+120+arg_0 , #	
51 78 24 28 81 48 84 60 58 42 24 28	<pre>ir (rspil8irarg_0), #DS14818 w ecs, (rspil8irarg_0)</pre>	
	q sca	I
91 19	ecs, 1	
01 ER 02 CA	ecs, 1 id ecs, eds	
C1 89 88	er era, a	
89 41 24 28	es [rspt18hterg_0], ets	
08 44 24 28 C1 58 93	ess, [rop+10veerg_0]	
C1 E8 03 59 44 24 28	w [rup+10h+erg_0], ess	
01 74 24 20 55 76 90 35	er [rap+10h+arg_0], 30907605h	
08 44 24 28	w saw, [repetitiong_0]	
89 44 24 28 48 83 CA 18	w [rsp+180+arg_0], man	
48 89 CA 18	to rop. 18h	
	b_10001A35C andp	

	8B	4C	24	38					mov	ecx, [rsp+18h+port_xor_v0]
-	8B	04	24						mov	eax, [rsp+18h+port_xor_v1]
	33	C8							xor	ecx, eax ; ecx = port_xor_v0 ^ port_xor_v1
	B8	25	49	92	24				mov	eax, 24924925h ; junk
	41	89	48	04					mov	[r8+4], ecx ; Stored to pointer output parameter
	C7	44	24	20	3D	4A	00	00	mov	[rsp+18h+arg 0], 4A3Dh
-	C1	6C	24	20	09				shr	[rsp+18h+arg 0], 9
	81	74	24	20	B1	A8	84	6D	xor	[rsp+18h+arg 0], 6D84A8B1h
	8B	4C	24	20					mov	ecx, [rsp+18h+arg 0]
	F7	E1							mul	ecx
	2B	CA							sub	ecx, edx
	D1	E9							shr	ecx, 1
	03	CA							add	ecx, edx

- port\_xor\_v0 ^ port\_xor\_v1 = 32-bit integer
- Stored to the output argument in <u>offset 4</u>.
- Encodes two 16-bit values:
  - offset 0x04: 0 if it's a decoy C2, 1 if real.
  - offset 0x06: The port integer in little-endian.



#### Extraction options

- Use regular expressions:
  - Junk code => unpredictability.
    - Inserted at compile-time.
    - Could break or interfere with regex patterns.
  - Risks:
    - We could extract wrong XOR parts (junk code).
    - New samples could change the XOR to an ADD or SUB etc.
    - Extractor logic may yield wrong but valid IPv4 addresses.

2.5	C7	44	24	30	82	27	96	65	mov	[rsp+18h+ip_xor_v1], 65962782h
	C7	04	24	8D	9C	09	32		mov	[rsp+18h+port_xor_v1], 32099C8Dh
	C7	44	24	28	AA	EC	A8	24	mov	[rsp+18h+ip_xor_v0], 24A8ECAAh
	C7	44	24	38	8D	9C	91	9B	mov	[rsp+18h+port_xor_v0], 9B919C8Dh



#### Extraction options

- Use Code Emulation:
  - Treat callbacks as gray-boxes:
    - Emulate the function's x64 instructions.
    - Read out the results from the emulator's memory.
  - Arithmetic operator changes will have no effect e.g. XOR, ADD, SUB



- We'll start by emulating a single function.
- We will automate the collection and emulation of all functions later on.

-		
	33 CØ	xon eax, eax
	4C 8B C1	mov r8, rcx ; Accepts a single argument in RCX
	89 44 24 0C	<pre>mov [rsp+18h+var_C], eax</pre>
	8B 4C 24 28	mov ecx, [rsp+18h+ip xor v0]
1	8B 44 24 30	mov eax, [rsp+18h+ip xor v1]
	33 C8	<pre>xor ecx, eax ; ecx = ip_xor_v0 ^ ip_xor_v1</pre>
	41 89 08	<pre>mov [r8], ecx ; Stored to pointer output parameter</pre>
	8B 4C 24 38	mov ecx, [rsp+18h+port xor v0]
1	8B 04 24	mov eax, [rsp+18h+port xor v1]
-	33 C8	<pre>xor ecx, eax ; ecx = port_xor_v0 ^ port_xor_v1 ; ecx &lt;= 16-bit port</pre>
	B8 25 49 92 24	mov eax, 24924925h ; junk
	41 89 48 04	mov [r8+4], ecx ; Stored to pointer output parameter



- Callbacks use the stack:
  - To store the artifact parts.
- We have to map memory for the stack in the emulator's memory.

89	44	24	0C	mov	[rsp-	+18h+var_C], eax	
8B	4C	24	28	mov	ecx,	[rsp+18h+ip_xor_v0]	
8B	44	24	30	mov		[rsp+18h+ip_xor_v1]	
8B	4C	24	38	mov		[rsp+18h+port_xor_v0]	
8B	04	24		mov	eax,	[rsp+18h+port_xor_v1]	

- Set RSP to point somewhere in the middle.
  - Stack grows downwards.



- Callbacks expect a single argument:
  - Output memory location.
  - Size: 8 bytes.
- We have to map a memory region for the output argument.
- Set RCX to its address.

41 89 08	mov	[r8], ecx	; Stored to poin	ter output paramet	ter

		41 89 48 04	mov	[r8+4], ecx	; Stored to	pointer output	parameter
--	--	-------------	-----	-------------	-------------	----------------	-----------



- Emulate the function.
- Read the function's output from the passed in argument:
  - Offset <u>0x00</u>: IPv4.
  - Offset <u>0x04</u>: Is real or decoy C2?
  - Offset <u>0x06</u>: Port.
  - Validate the IP and port and format into a C2: o e.g. "https://129.232.188.93:443"

0x00	0x04	0x06
IPv4 address (network-byte order aka big-endian)	Is Real C2? (little-endian)	Port (little-endian)
4 bytes	2 bytes	2 bytes



•

## Extracting all controllers

• Find all callbacks and emulate each one of them.



## Steps

- Step 1: Find possible callback functions using a regular expression.
- Step 2: Validate them by examining the disassembly.
  - Must have a single basic block.
    - No jumps.
  - Must not call to another function.
- Step 3: Emulate validated callbacks.



## Steps

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## Steps

- Step 1: Find possible callback functions using a regular expression. ۲
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  - Must have a single basic block.
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- Step 3: Emulate validated callbacks 🔽  $\bullet$





#### Step 1: Find possible callbacks

- A <u>LEA</u> instruction loads the address of each callback function into a 64-bit register.
- Create a regex to match this pattern across the whole binary.
- We only want to process references to code.
  - Validate match and xref are in the same section.
- Will still match functions that are not C2 callbacks.
  - Filtered out in the next step.

_									V
۲	4	X							
								init c	allback table:
48	8D	05	06	7E	01	00		lea	rax, callback_48
48	89	85	C0	00	00	00		mov	[rbp+150h+var 90], rax
48	8D	05	10	2D	02	00	[	lea	rax, callback 5
48	89	44	24	68				mov	[rsp+250h+var_1E8], rax
C7	85	68	01	00	00	2C	F3	mov	[rbp+150h+arg_8], 0F32Ch
00	00								
6B	85	68	01	00	00	6D		imul	eax, [rbp+150h+arg_8], 6Dh ; 'm
89	85	68	01	00	00			mov	[rbp+150h+arg 8], eax
81	B5	68	01	00	00	D8	89	xor	[rbp+150h+arg_8], 6789D8h
67	00								
8B	85	68	01	00	00			mov	eax, [rbp+150h+arg 8]
89	85	68	01	00	00			mov	[rbp+150h+arg 8], eax
48	8D	05	3B	64	01	00	- [	lea	rax, callback 23
48	89	45	F8					mov	[rbp+150h+var 158], rax
C7	85	68	01	00	00	D5	4D	mov	[rbp+150h+arg_8], 4DD5h
00	00								
C1	AD	68	01	00	00	0C		shr	[rbp+150h+arg_8], 0Ch
C1	A5	68	01	00	00	0A		shl	[rbp+150h+arg_8], 0Ah
C1	AD	68	01	00	00	0B		shr	[rbp+150h+arg 8], 0Bh
83	B5	68	01	00	00	66		xor	[rbp+150h+arg_8], 66h
8B	85	68	01	00	00			mov	eax, [rbp+150h+arg_8]
89	85	68	01	00	00			mov	[rbp+150h+arg 8], eax
48	8D	05	7E	C5	01	00	- [	lea	rax, callback 39
48	89	45	78					mov	[rbp+150h+var D8], rax

File: "IDBs/emotet/emotet\_0.bin.i64" Disassembly at 0x1800030DF



## Step 2: Validating callbacks

- Step 1: Find possible callback functions using a regular expression.
- Step 2: Validate them by examining the disassembly.
  - Must have a single basic block.
    - No jumps.
  - Must not call to another function.
- Step 3: Emulate validated callbacks.



#### Capstone engine

- Lightweight multi-platform, multi-architecture disassembly framework.
- Intuitive and easy-to-use API to disassemble and analyze instructions.
- Actively maintained, used by projects such as Radare2.
- Easy to install: "pip install capstone"



www.capstone-engine.org



#### Capstone engine

- Learn more about Capstone capabilities:
  - <u>https://github.com/capstone-engine/capstone/blob/next/bindings/python/test\_x86.py</u>



#### Step 3: Emulate validated callbacks

• Already done that earlier in this section.



## Conclusion

- Malware evolves and changes are unpredictable.
- The extractor will break but things can be done to minimize that:
  - Anticipate changes e.g. generic regex.
  - Rely on the static parts when possible. Example:
    - Check many versions, see what doesn't change in/around an area you want to locate.
    - Chances are future versions are the same.
- It is better for the extractor to register nothing than to yield wrong IOCs.
  - Perform sanity checks.
  - Log extensively to help with debugging.



## Appendix 1: Mapping PE to Unicorn Memory

Emulating code that calls into other functions and/or accesses its data sections would require mapping the PE executable into the emulator's memory. Writing the raw PE file to memory, as it is on disk, would lead to invalid relative offsets and memory accesses since the alignment of PE sections in the physical file differs from their alignment in memory. To map a PE to Unicorn engine's memory:

# load PE file.
pe = pefile.PE(pe\_path)

# Get memory-mapped PE image. pe\_img = pe.get\_memory\_mapped\_image()

# Get the image base address. img\_base = pe.OPTIONAL\_HEADER.ImageBase

# Initialize Unicorn
emulator = unicorn.Uc(unicorn.UC\_ARCH\_X86, unicorn.UC\_MODE\_32)

# Map memory for the PE at the image base. The image size is aligned to page boundary. emulator.mem\_map(img\_base, (len(pe\_img) + 0xfff) & ~0xfff)

# Write the memory-mapped image to the emulator's memory at the image base. emulator.mem\_write(img\_base, pe\_img)



### Appendix 2: Unicorn engine hooks

The Unicorn engine is OS-agnostic, and so emulating code will inevitably lead to exceptions or undefined behavior. Luckily the engine offers useful hooks for the developer to correct the behavior or implement workarounds. The implementation details are largely tied to specific use-cases hence why these hooks are user-defined.

One notable hook - that we find ourselves registering a lot - is the <u>invalid memory access hook</u>. It is a function that gets invoked when the emulated instruction causes an invalid memory access. The hook would attempt to resolve this access by mapping the memory at the faulting address and returning 'True'. In which case, the Unicorn engine would re-execute the instruction and continue emulation. On the other hand, emulation would stop when the hook returns 'False'.

def uc\_invalid\_mem\_access\_hook(emulator, access\_type, address, size, value, \_user\_data): # Align to previous page boundary and map e.g. address 0x20098 becomes 0x20000. emulator.mem\_map(address & ~0xfff, 0x1000) return True

# Initialize the emulator and register the hook emulator = unicorn.Uc(unicorn.UC\_ARCH\_X86, unicorn.UC\_MODE\_32) emulator.hook\_add(unicorn.UC\_HOOK\_MEM\_INVALID, uc\_invalid\_mem\_access\_hook)



## Appendix 2: Unicorn engine hooks

The code hook is another useful callback that you will usually need to implement. A major drawback is that it slows down the emulation speed considerably because the engine breaks out to invoke the user-defined function prior to the execution of every instruction.

The example below uses this hook to skip all call instructions in the emulated code with the help of Capstone.

# Initialize Capstone
cap\_md = capstone.Cs(capstone.CS\_ARCH\_X86, capstone.CS\_MODE\_32)
cap\_md.detail = True

def uc\_code\_hook(emulator, address, size, user\_data):
 try:
 # Read and disassemble the instruction
 inst = next(cap\_md.disasm(emulator.mem\_read(address, size), 0))
 except StopIteration:
 return
 # If it's a CALL instruction skip it
 if inst.id == capstone.x86.X86\_INS\_CALL:
 emulator.reg\_write(unicorn.x86\_const.UC\_X86\_REG\_EIP, address + size)

# Initialize Unicorn and register the code hook emulator = unicorn.Uc(unicorn.UC\_ARCH\_X86, unicorn.UC\_MODE\_32) emulator.hook\_add(unicorn.UC\_HOOK\_CODE, uc\_code\_hook)



# Thank you!

@Dark\_Puzzle  $\mathbb{X}$ 

